Institut de Ciències del Cosmos

# Low noise 4 channel with On-Chip DLL for calorimetric detector readout

Data Sheet **ICECALv3**

## FEATURES

4 fully differential analog channels with cooled active impedance termination (no 50Ω resistor needed) for reduced noise.

DLL for each channel to help synchronize at 40MHz.

Digital interface using SPI protocol.

Dynamic range: 12 bits

Low input referred noise < 1 nV/√Hz

Relative linearity error: < 1%

Signal stable (< 1% variation) for > 4 ns

Spill-over < 1%

Input range: ?? mAp

Single-ended input to differential output

3.3 V supply

## APPLICATIONS

Photodetectors readout.

## GENERAL DESCRIPTION

The ICECALv3 includes: four analog channels with programmable values to control the key parameters and compensate for process variations; a dedicated DLL to synchronize each channel signal phase (compensate for channel to channel differences due to different PMT voltages and cable lengths) and a digital interface using SPI protocol.

The ICECALv3 is developed by using the Austria Micro Systems (AMS) 0.35 µm SiGe BiCMOS technology and operates over the −40°C to +125°C junction temperature range. The ICECALv3 is available in a 64-QFN package.

## TYPICAL APPLICATION CIRCUIT

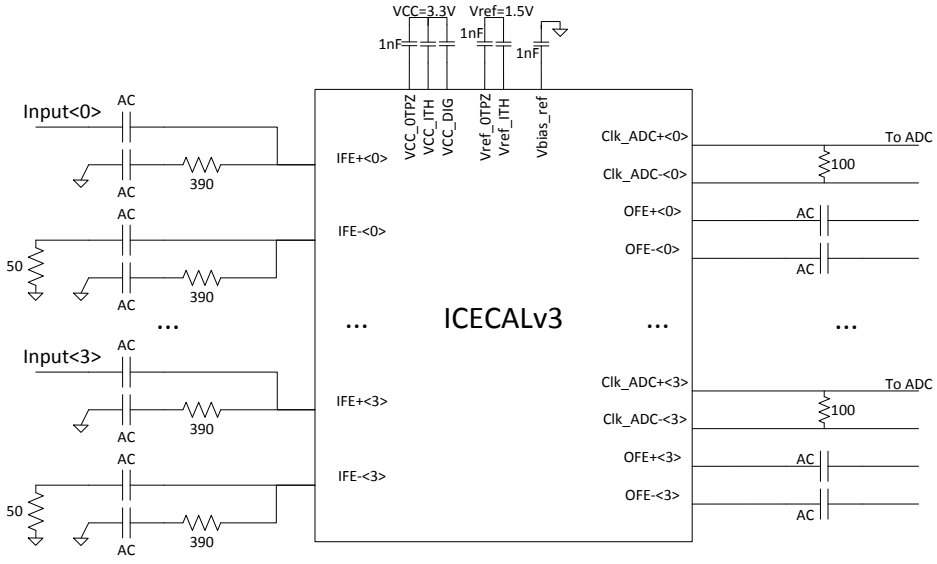



*Figure 1: ICECALv3 Typical application circuit*

**Rev. 3**



**Av. Diagonal 645, Barcelona, ES 08028, SPAIN**
**Tel: 93.40.21588**
**Fax: 93.40.21241**
**icc.ub.edu**

# TABLE OF CONTENTS



# REVISION HISTORY

**4/14—Revision 0: Initial Version**
**17/03/2015—Revision 0.5: Table 4 errors fixed**
**24/01/2018—Revision 0.12: Soft reset changed to 0x50.**

[1] Coaxial cable connection between the PMT output and the preamplifier input.

## FUNCTIONAL BLOCK DIAGRAM

The analog channel is designed with an input amplifier that includes an electronically cooled termination input stage with double feedback. A passive line termination would induce too large a noise and is avoided. Afterwards an alternated switched differential signal paths scheme permits the integration of the signal with no dead time between consecutive events. Each path includes a pole-zero filter in order to compensate for cable effects, a switched integrator with capacitive feedback, a Track-and-hold for a 12-bit ADC, and a MUX to select the correct sub-channel output signal. A fully differential signal processing is adopted in order to minimize the impact of common mode noise, which is important in a switched system.

Each analog channel includes a delay line based on a Delay Locked Loop (DLL) so the user can set a delay to compensate the delay introduced, for example, by PMT voltage settings or cable lengths. The DLL is adjusted by means of two control voltages to ensure that systematic process or environmental variations will not affect the channel time tuning. A fully differential design of the DLL aims at reducing the switching noise produced by delay lines. The clock jitter induced by transient noise is lower than 4ps.

The design of this chip prototype is also determined by the radiation environment. The design must tolerate SEUs, SETs and SELs. The probability of SELs is reduced by increasing the distance between PMOS and NMOS transistors and inserting double guard rings between them, so that PMOS and NMOS transistors are confined inside islands of the same transistor type. SEUs are avoided by implementing Triple Modular Redundancy Registers to store the DLL configuration and fault tolerant Finite State Machine in the SPI Slave. Finally, reset signals are protected from SETs by means of glitch suppressors.

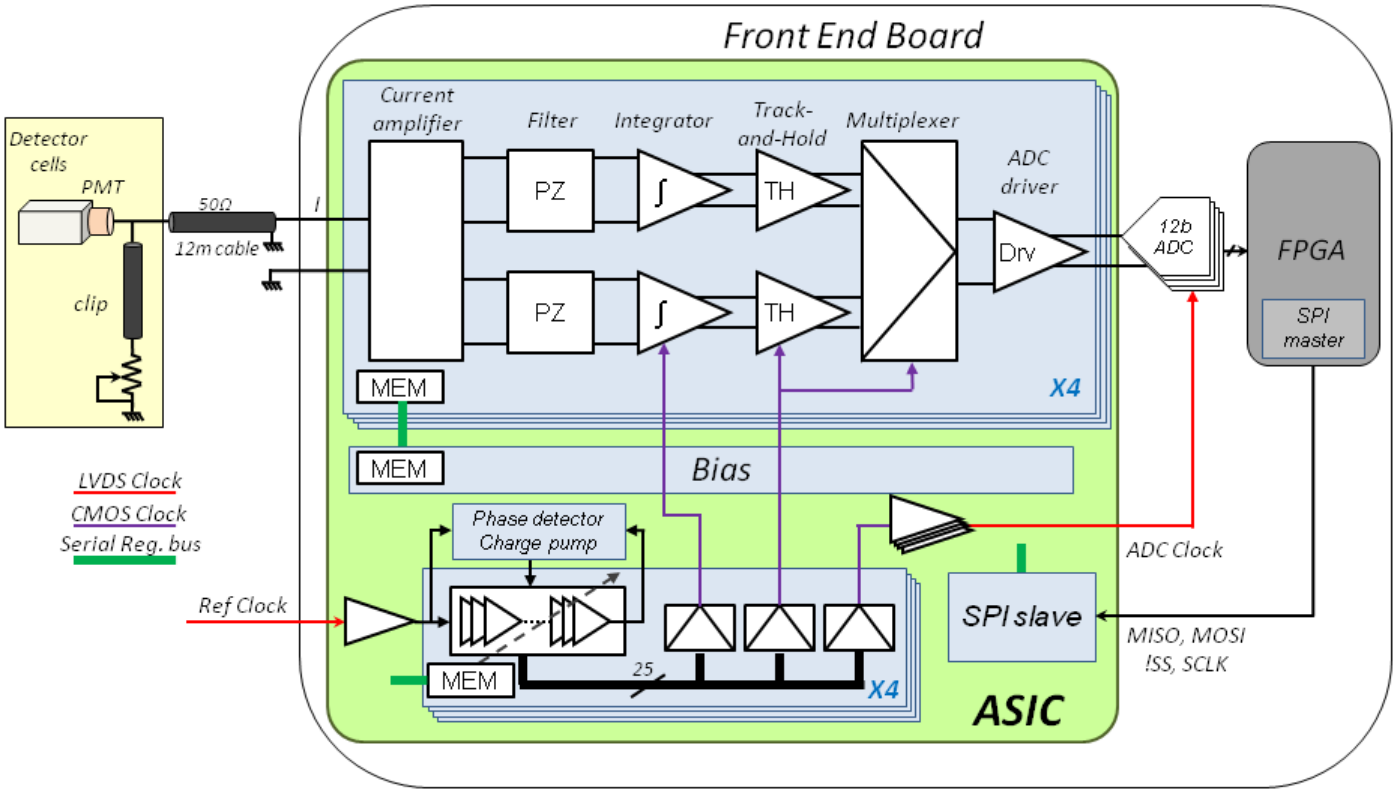



*Figure 2: ICECAL Functional Block Diagram*

# SPECIFICATIONS

$T_A$ = +25°C, $V_{CC\_0TPZ}$ = 3.3 V, $V_{CC\_ITH}$ = 3.3 V, $V_{CC\_DIG}$ = 3.3 V.

**Table 1**

| Parameters | Conditions [1] | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| SLOW CONTROL PARAMETERS | | | | | |
| SPI frequency | MISO pull-up resistor = 500 Ω | | 10 | | MHz |
| DELAY LINE | | | | | |
| Clock steps | | 0.995 | 1.000 | 1.005 | ns |
| LVDS ADC Output Clock current | | 0.35 | 3.0 | 3.0 | mA |
| LVDS Common Mode voltage | | | 1200 | | mV |
| LVDS Differential Mode voltage | Termination resistor = 100 Ω | ±35 | ±150 | ±150 | mV |
| Clock Jitter | | | 5 | | ps |
| Differential Non-Linearity (DNL) | | | 23 | | ps rms |
| $V_{coarse}$ | | 1.0 | 1.9 | 3.3 | V |
| DYNAMIC PERFORMANCE | | | | | |
| Calibration | | | 4 | | fC/LSB |
| Dynamic Range | | | 12 | | Bits |
| Input charge | | 0 | | | C |
| Output voltage | | 0 | | 2 | V |
| Output ADC | | 256 | | 4096 | ADCcounts |
| INPUT | | | | | |
| Relative Linearity Error (charge) | Nonlinearity | | < ± 1% | | phe |
| Max Input Current Range [1] | Saturation | | 290 | | µA |
| NOISE | | | | | |
| Input Referred Noise | | | 1 | | nV/√Hz |
| Total Output RMS Noise | | | 1.6 | | LSB rms |
| OUTPUT | | | | | |
| Differential Offset | | | | | mV |
| Output Common-Mode Voltage | | | | | V |
| Voltage Swing (Differential) | | 0 | | 2 | V |
| POWER SUPPLY | | | | | |
| Input Voltage | | 3.2 | 3.3 | 3.4 | V |
| Current | $V_{cc}$ | | | | mA |
| Power Dissipation [4] | $V_{cc}$ = 3.3 V | | | | mW |

# ABSOLUTE MAXIMUM RATINGS

**Table 2**

| Parameter | Rating |
|---|---|
| $V_{CC\_0TPZ}$ | 3.2 V to 3.4 V |
| $V_{CC\_ITH}$ | 3.2 V to 3.4 V |
| $V_{CC\_DIG}$ | 3.2 V to 3.4 V |
| $V_{CM}$ | 1.3 V to 1.9 V |
| $V_{ref}$ | 1.4 V to 1.9 V |
| Temperature Range | |
| Operating (Junction) | −40°C to +125°C |
| Storage | −65°C to +150°C |
| Soldering Conditions | JEDEC J-STD-020 |

1 A voltage regulator needs to be added to provide the $V_{ccb}$ voltage. The baseline for the regulator chip is ADP161.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

## BOUNDARY CONDITION

$\theta_{JA}$ is measured using natural convection on a JEDEC 4-layer board, and the exposed pad is soldered to the printed circuit board (PCB) with thermal vias.

**Table 3: Thermal Resistance**

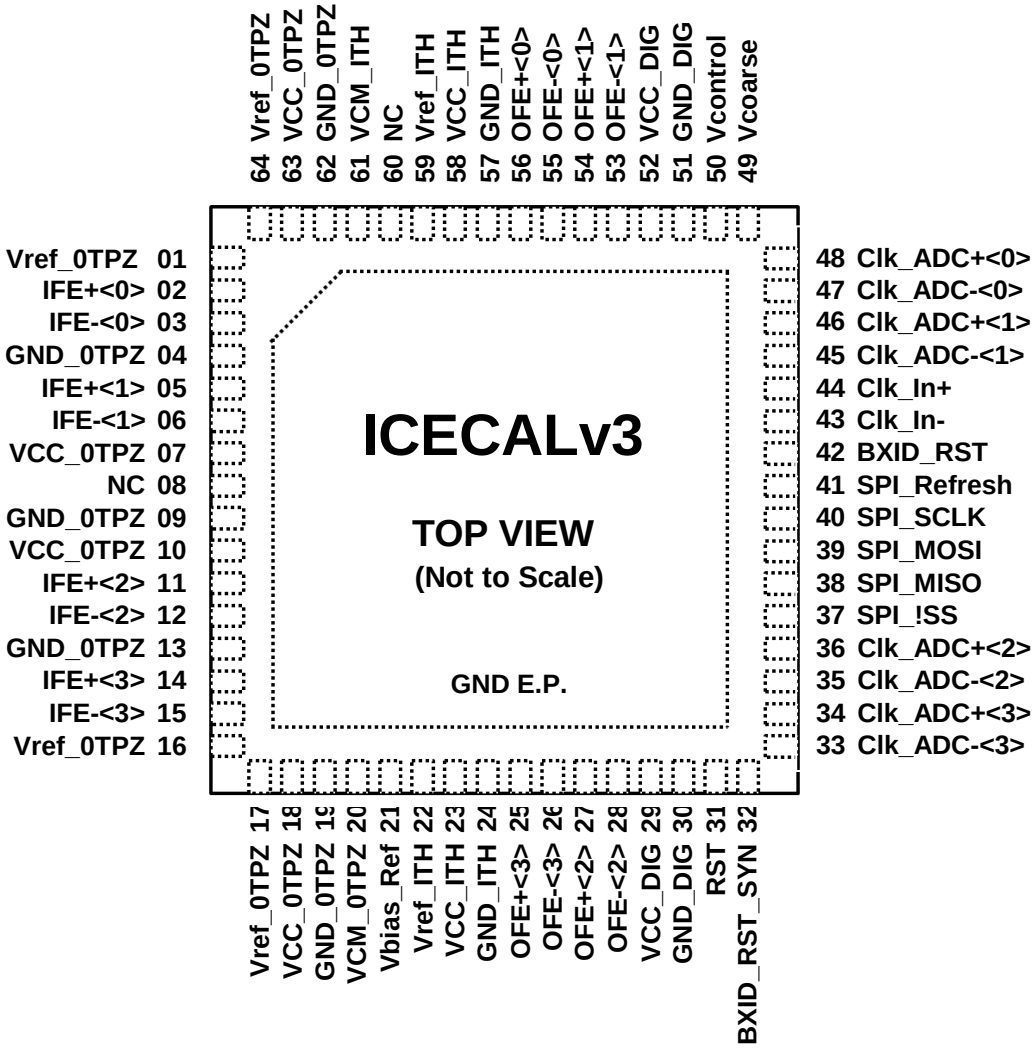
| Package Type | $\theta_{JA}$ | Unit |
|---|---|---|
| 64-Lead QFN | TBC [1] | °C/W |

[1] To be confirmed.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS




**NOTES 1. THE EXPOSED PAD SHOULD BE SOLDERED TO AN EXTERNAL GND PLANE.**

*Figure 3: Figure 3. Pin Configuration (Top View)*

**Table 4: Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 16, 17, 64 | $V_{Ref\_0TPZ}$ | 0T and Pole/Zero voltage reference. |
| 2, 5, 11, 14 | $I_{FE}$+<0:3> | Noninverting differential Input. Typically ac-coupled. |
| 3, 6, 12, 15 | $I_{FE}$-<0:3> | Inverting differential Input. Typically ac-coupled. |
| 4, 9, 13, 19, 62 | $GND_{0TPZ}$ | Exposed Pad is internally connected to GND and must be soldered to a low impedance ground plane. |
| 7, 10, 18, 63 | $VCC_{0TPZ}$ | Positive 3.3 V power supply for 0T and Pole/Zero. |
| 8, 60 | NC | Not connected. |
| 20 | $V_{CM\_0TPZ}$ | 0T and Pole/Zero Common Mode Voltage. |
| 21 | $V_{Bias\_Ref}$ | Bias voltage of the chip to be connected to a decoupling capacitor. |
| 22, 59 | $V_{Ref\_ITH}$ | Integrator and Track&Hold voltage reference. |
| 23, 58 | $V_{CC\_ITH}$ | Positive 3.3 V power supply for Integrator and Track&Hold. |
| 24, 57 | $GND_{ITH}$ | Exposed Pad is internally connected to GND and must be soldered to a low impedance ground plane. |
| 25, 27, 54, 56 | $O_{FE}$+<3:0> | Noninverting differential Ouput. Typically ac-coupled. |
| 26, 28, 53, 55 | $O_{FE}$-<3:0> | Inverting differential Output. Typically ac-coupled. |
| 29, 52 | $V_{CC\_DIG}$ | Positive 3.3 V power supply for the digital blocks (slow control and delay line). |
| 30, 51 | $GND_{DIG}$ | Exposed Pad is internally connected to GND and must be soldered to a low impedance ground plane. |
| 31 | RST | Chip reset (active high). Resets the SPI interface, restores the default value of serial registers and resets the charge pump of the delay line. |
| 32 | $BXID_{RST\_SYN}$ | Outputs the BXID synchronous reset signal resynchronized by the input reference clock. For testing purposes. |
| 33, 35, 45, 47 | $Clk_{ADC}$-<3:0> | Inverting LVDS Output Clock to synchronize the external ADC data sampling. A termination resistor of 100 Ω is required between inverting and noninverting pins. |
| 34, 36, 46, 48 | $Clk_{ADC}$+<3:0> | Noninverting LVDS Output Clock to synchronize the external ADC data sampling. A termination resistor of 100 Ω is required between inverting and noninverting pins. |
| 37 | $SPI_{!SS}$ | SPI slave select. Input signal. Active low. |
| 38 | $SPI_{MISO}$ | SPI Master Input / Slave Ouptut. External pull-up resistor of 500 Ω. |
| 39 | $SPI_{MOSI}$ | SPI Master Output / Slave Input. |
| 40 | $SPI_{SCLK}$ | SPI Serial Clock. Input signal. |
| 41 | $SPI_{Refresh}$ | SPI Auxiliary Clock. Used to refresh TMR registers and correct SEUs (if any) during data taking. Input signal. |
| 42 | $BXID_{RST}$ | BXID synchronous reset signal that allows sub-channel identification. Input signal. |
| 43 | $Clk_{In}$- | Inverting LVDS Input Clock reference. |
| 44 | $Clk_{In}$+ | Noninverting LVDS Input Clock reference. |
| 49 | $V_{Coarse}$ | Delay line external coarse adjust. Input signal. |
| 50 | $V_{Control}$ | Delay line internally generated control voltage. Output signal. For testing purposes. |
| 61 | $V_{CM\_ITH}$ | Integrator and Track&Hold Common Mode Voltage. |

# DIGITAL DELAY LINE

As observed in Figure 2, each of the four ASIC channels requires three independent adjustable clocks: one for the pulse integration, a second for the analog sampling and sub-channel multiplexing and a third for the external digitizing.

The integration and analog sampling procedure require an adjustable clock to cope with the timing uncertainty of the input signal pulses. This uncertainty is caused by the length of signal cables and the dispersion of scintillating fibers. Therefore, in order to digitize the analog sampled data when they are stable (plateau), external ADCs also require an adjustable clock.

## DELAY LINE CONFIGURATION

The basic delay element is shown in Figure 4. It consists in a current starved inverter where delay can be adjusted by controlling VCoarse and VControl.

VControl is automatically generated by an internal charge pump of the phase detector and it can be debugged by probing the pin number 50 (assuming that !VControl_EN is active. For more details, see Tables 14 and 15). Despite VControl cannot be modified, the internal charge pump can be fully discharged by sending a software reset through the SPI interface.

VCoarse is an externally generated fixed voltage that biases the delay line to the working frequency. To achieve the best performance in terms of jitter and linearity, the following equality should be satisfied:

VCoarse = VCC_DIG - VControl

Each Delay Line channel has a 16-bit TMR configuration register. Register addresses can be seen in Table 7 and configuration parameters are described in Table 17.

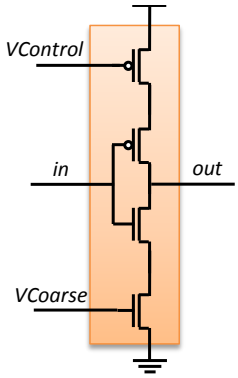



*Figure 4: Current starved inverter*

## SYSTEM SYNCHRONIZATION

The synchronization of the system consists in setting four phases values (one per chip and the others per channel). As shown in Figure 5, the minimum block to synchronize is composed by one ICECAL chip, ADCs for four channels, an FPGA to capture the data and control the ICECAL chip. If the minimum block is repeated in the same PCB design, the relative phases ($\Phi_{ICECAL\_CLK\_IN}$, $\Phi_{ADC}$ and $\Phi_{ADC\_FPGA}$) can be known for each integration time ($\Phi_{TH}$). Therefore, the synchronization procedure will be done varying only the integration phase (related to the maximum signal and spill-over) while all the rest of phases will be automatically set using a Look-Up-Table (LUT).

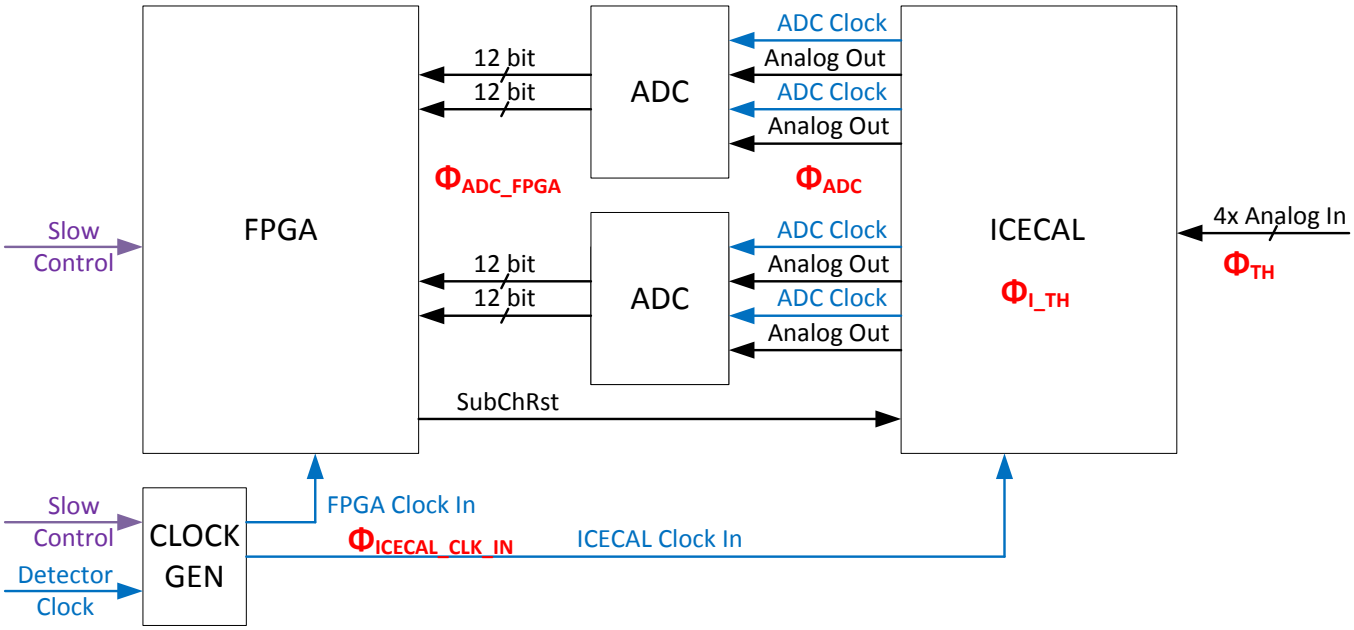



*Figure 5: System synchronization phases, clocks and signals.*

The method to develop the LUT of each phase depends on the signals to be synchronized:

1. **$\Phi_{ICECAL\_CLK\_IN}$**: This phase is defined by the global clocks that feed the FPGA and the ICECAL. Let us assume the clock phase of the FPGA is fixed. Then, the *SubChRst* signal will be captured correctly for some of the phases of the ICECAL clock. The $\Phi_{ICECAL\_CLK\_IN}$ must be placed in the most stable phase for which the sub-channel reset is performed. It can be fixed beforehand as it will be the same for each PCB design.
2. **$\Phi_{I\_TH}$** is defined as the delay between the integration time and the Track-and-Hold clocks. It only depends on the internal delays of the chip and its optimal value has been measured to be 1ns.
3. **$\Phi_{TH}$**: each channel of the detector will have a different optimum integration time mainly due to differences in particle time arrival, PM high voltage biasing and signal cable length. The channel integration time is defined by the TH phase minus $\Phi_{I\_TH}$, which is already fixed. Consequently, the TH phase defines the signal integration time and has to be tuned at the detector. The method for $\Phi_{TH}$ can include look for the maximum signal and minimum spill over.
4. **$\Phi_{ADC}$**: the ADC phase is used to select the time at which the ADC performs the conversion of each ICECAL analog channel output. In principle it should be a fixed value to be added to the TH phase. It only depends on the PCB design. A LUT can be prepared for each $\Phi_{TH}$. A first approximation for this value can be found using a scope on the ICECAL analog output because the ADC switching is clearly visible.
5. **$\Phi_{ADC\_FPGA}$**: as in the ADC phase, the ADC 12 bits of data have to be captured by the FPGA in parallel at the right phase or there will be data corruption. There is no dedicated clock signal but the data can be captured at the rising or falling edge of the FPGA clock. As in the previous case, the relative phase only depends on the PCB design, so, for a board design, a LUT with the rising or falling edge, depending on the $\Phi_{TH}$ can be prepared.

# SPI INTERFACE

Slow control for the device is implemented using a standard SPI (Serial Peripheral Interface) signals and protocol. This interface permits to read/write the ICECAL internal registers.

## DATA TRANSMISSION

As observed in Figure 4, each SPI frame consists in 3 bytes: 1 byte for addresses or commands and 2 bytes for data. The first bit in the transmission determines the data direction (read/write). When low, data is written to the selected register through MOSI pin while previous data can be read simultaneously from MISO pin (R+W operation). When high, data is read from the MISO pin (RO operation).

## REGISTER ADDRESSES AND FUNCTIONALITY

The 8-bit SPI address frame is as follows:

*Table 5: SPI address frame*

| $b_7$ | $b_6$ | $b_5$ | $b_{4..0}$ |
|---|---|---|---|
| R/!W | $PUMP_{RST}$ | !CONF | $REG_{SEL}$<4:0> |

There are different types of slow control frames according to the SPI address:

- Soft reset command.
- SPI bypass command.
- Status register access (RO).
- Configuration register access (RO / R+W).
  - ICECAL Channel configuration.
  - Delay Line Channel configuration.
  - Global configuration.

*Table 6: Slow control frame types according to the SPI address bits*

| Description | R/!W | $PUMP_{RST}$ | !CONF | $R_{SEL}$<4:0> |
|---|---|---|---|---|
| Soft Reset | 0 | 1 | 0 | 0x10 |
| SPI Bypass | 1 | 1 | 1 | 0x1F |
| Status Register | 1 | 0 | 1 | X |
| Config. Register | X | 0 | 0 | X |

When software reset command is issued, the internal charge pump which controls delay lines is reset, and therefore, this will force the delay lines to be resynchronized with the reference clock. This is useful to recover delay lines without a hard reset (which implies register data configuration loss).

The SPI bypass message command loopbacks MOSI and MISO lines during the transmission of the next 16 data bits. This message eases the troubleshooting procedure.

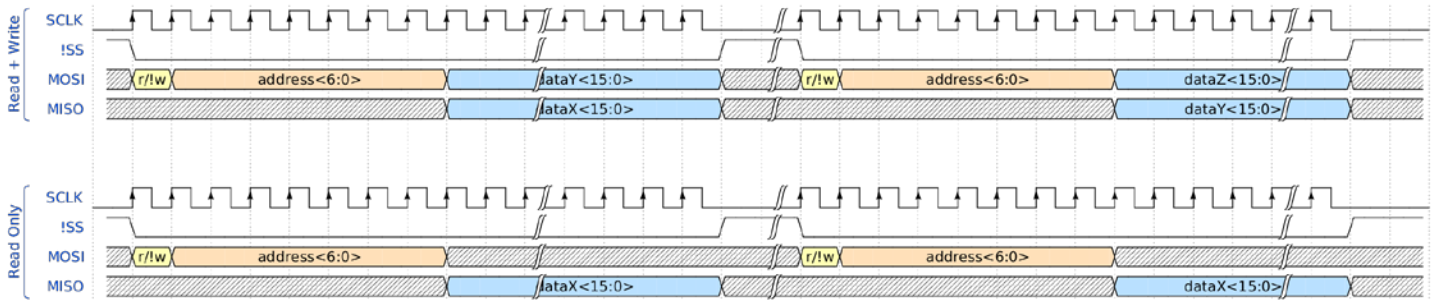



*Figure 6: An example of register read+write access (top) and register read only access (bottom).*

Status registers provide information about the ICECAL operation and they can only be read (write+read commands will be ignored).

*Table 7: Status registers address mapping*

| Description | R/!W ($b_7$) | PUM PRST ($b_6$) | !CONF ($b_5$) | REG SEL <4:0> ($b_{4:0}$) | Default |
|---|---|---|---|---|---|
| ICECAL version | 1 | 0 | 1 | X10 | Bits <15:12> major revision number.<br>Bits <11:8> minor revision number. |
| BXID resynch | 1 | 0 | 1 | X11 | Bit 15 returns 1 if the synchronous $BXID_{RESET}$ signal (pin 42) is being properly resynchronized with the input clock. |

*Table 8: Configuration registers address mapping*

| Description | R/!W ($b_7$) | PUM PRST ($b_6$) | !CONF ($b_5$) | REG SEL <4:0> ($b_{4:0}$) | Default |
|---|---|---|---|---|---|
| ICECAL Ch0<15:0> | X | 0 | 0 | X00 | 0x2913 |
| ICECAL Ch1<15:0> | X | 0 | 0 | X01 | 0x2913 |
| ICECAL Ch2<15:0> | X | 0 | 0 | X02 | 0x2913 |
| ICECAL Ch3<15:0> | X | 0 | 0 | X03 | 0x2913 |
| ICECAL Ch0<31:16> | X | 0 | 0 | X04 | 0x7FA0 |
| ICECAL Ch1<31:16> | X | 0 | 0 | X05 | 0x7FA0 |
| ICECAL Ch2<31:16> | X | 0 | 0 | X06 | 0x7FA0 |
| ICECAL Ch3<31:16> | X | 0 | 0 | X07 | 0x7FA0 |
| ICECAL Main<15:0> | X | 0 | 0 | X08 | 0x479C |
| ICECAL Main<31:16> | X | 0 | 0 | X09 | 0x345E |
| ICECAL Main<47:32> | X | 0 | 0 | X0A | 0x079E |
| ICECAL Main<63:48> | X | 0 | 0 | X0B | 0x0A67 |
| Delay Line Ch0 | X | 0 | 0 | X1C | 0x0011 |
| Delay Line Ch1 | X | 0 | 0 | X1D | 0x0011 |
| Delay Line Ch2 | X | 0 | 0 | X1E | 0x0011 |
| Delay Line Ch3 | X | 0 | 0 | X01F | 0x0011 |

Configuration registers (see Table 8) store adjustable parameters of the electronics. In order to avoid SEUs, these registers are implemented using Triple Modular Redundancy (TMR).

## REGISTER DATA

In the following tables it is defined the bits and corresponding functionality for all the registers in the chip.

Table 9 and Table 10 define the Chip version register.

*Table 9: ICECAL version status register (Address 0xB0)*

| $D_{15..12}$ | $D_{11..8}$ | $D_{7..0}$ |
|---|---|---|
| MAJOR | MINOR | - |

*Table 10: ICECAL version status register bits function*

| Bits | Function |
|---|---|
| MAJOR | ICECAL major revision number. |
| MINOR | ICECAL minor revision number. |

*Table 11: BXID resynch status register (Address 0xB1)*

| $D_{15}$ | $D_{14..0}$ |
|---|---|
| DETECTED | - |

*Table 12: BXID resynch status register bits function*

| Bits | Function |
|---|---|
| DETECTED | Returns 1 if the synchronous $BXID_{RST}$ signal (pin 42) is being properly resynchronized with the input reference clock (pins 43 and 44). |

Table 13 and Table 14 show the channel control register bits. Each of the analog channels contains the corresponding register for programmable values to control the key parameters and compensate for process variations. It is possible to vary the values of the input impedance, the pole and zero frequencies of the PZ filter and the integrator capacitor (for gain variations).

*Table 13: ICECAL channel control register (hexadecimal default value = 7F-A0-29-13)*

| $D_{31..30}$ | $D_{29..27}$ | $D_{26..24}$ | $D_{23..20}$ | $D_{19..18}$ | $D_{17..16}$ |
|---|---|---|---|---|---|
| $Cint_{MSB}$ | $Cint_{LSB0}$ | $Cint_{LSB1}$ | $IOff_{MSB}$ | $IOff_{LSB0}$ | $IOff_{LSB1}$ |
| $D_{15..11}$ | $D_{10..5}$ | $D_{4..0}$ | | | |
| Zero | Pole | $Z_{In}$ | | | |

*Table 14: ICECAL channel control register bits function (hexadecimal default value = 7F-A0-29-13)*

| Bits | | Default | Function |
|---|---|---|---|
| $Cint_{MSB}$ | $D_{31..30}$ | 0x1 | Integrator capacitor 2 MSB common for both sub-channels |
| $Cint_{LSB0}$ | $D_{29..27}$ | 0x7 | Integrator capacitor 3 LSB for sub-channel 0 only |
| $Cint_{LSB1}$ | $D_{26..24}$ | 0x7 | Integrator capacitor 3 LSB for sub-channel 1 only |
| $IOff_{MSB}$ | $D_{23..20}$ | 0xA | Offset current 4 MSB common for both sub-channels |
| $IOff_{LSB0}$ | $D_{19..18}$ | 0x0 | Offset current 2 LSB for sub-channel 0 only |
| $IOff_{LSB1}$ | $D_{17..16}$ | 0x0 | Offset current 2 LSB for sub-channel 1 only |
| Zero | $D_{15..11}$ | 0x5 | Capacitor bits for the zero of the PZ filter. Zero frequency ranges from 12.84 MHz to 42.78 MHz. |
| Pole | $D_{10..5}$ | 0x8 | Capacitor bits for the pole of the PZ filter. Pole frequency ranges from 13.10 MHz to 106.10 MHz. |
| $Z_{In}$ | $D_{4..0}$ | 0x13 | Input impedance control |

The main control register of the chip (Table 15 and Table 16) is essentially used for bias currents for the operational amplifier at different stages and the input preamplifier and it is shared by the four analog channels.

*Table 15: ICECAL main control register (hexadecimal default value = 0A-67-07-9E-34-5E-47-9C)*

| $D_{63}$ | $D_{62}$ | $D_{61}$ | $D_{60}$ | $D_{59..54}$ |
|---|---|---|---|---|
| $!V_{Control\_EN}$ | $!BXID_{Syn\_EN}$ | $!Clk_{Refresh\_EN}$ | - | $I_{Bias\_OB}$ |
| $D_{53..48}$ | $D_{47..44}$ | $D_{43..38}$ | $D_{37..32}$ | $D_{31}$ |
| $I_{Bias\_CETH}$ | - | $I_{Bias\_TH}$ | $I_{Bias\_INT}$ | - |
| $D_{30..28}$ | $D_{27..22}$ | $D_{21..16}$ | $D_{15}$ | |
| $I_{Bias\_CEINT\_H}$ | $I_{Bias\_CEPZ}$ | $I_{Bias\_0T}$ | - | |
| $D_{14..12}$ | $D_{11..6}$ | $D_{5..0}$ | | |
| $I_{Bias\_CEINT\_L}$ | $I_{Bias\_PZ}$ | $I_{Bias\_V0T}$ | | |

*Table 16: ICECAL main register bits function and default values (hexadecimal default value = 0A-67-07-9E-34-5E-47-9C)*

| Bits | | Default | Function |
|---|---|---|---|
| $!V_{Control\_EN}$ | $D_{63}$ | 0x0 | This bit enables/disables control voltage output pin (59). Active low |
| $!BXID_{Syn\_EN}$ | $D_{62}$ | 0x0 | Enables or disables the output debug pin $BXID_{RST\_SYN}$ (32). Active low. |
| $!Clk_{Refresh\_EN}$ | $D_{61}$ | 0x0 | Enables or disables clock refresh of the TMR registers. If enabled, auxiliary clock pulses coming from $SPI_{Refresh}$ pin (41) will be forwarded to the serial registers while SPI slave is idle. Otherwise, two consecutive SEUs on the same TMR register might cause data corruption. Active low. |
| | $D_{60}$ | | Not used |
| $I_{Bias\_OB}$ | $D_{59..54}$ | 0x29 | Output buffer bias |
| $I_{Bias\_CETH}$ | $D_{53..48}$ | 0x27 | Track-And-Hold OpAmp bias |
| | $D_{47..44}$ | | Not used |
| $I_{Bias\_TH}$ | $D_{43..38}$ | 0x1E | Track-And-Hold OpAmp bias |
| $I_{Bias\_INT}$ | $D_{37..32}$ | 0x1E | Integrator OpAmp bias |
| | $D_{31}$ | | Not used |
| $I_{Bias\_CEINT\_H}$ | $D_{30..28}$ | 0x3 | 3 MSB of the integrator OpAmp bias |
| $I_{Bias\_CEPZ}$ | $D_{27..22}$ | 0x11 | Pole-Zero OpAmp bias |
| $I_{Bias\_0T}$ | $D_{21..16}$ | 0x1E | 0T bias |
| | $D_{15}$ | | Not used |
| $I_{Bias\_CEINT\_L}$ | $D_{14..12}$ | 0x4 | 3 LSB of the integrator OpAmp bias |
| $I_{Bias\_PZ}$ | $D_{11..6}$ | 0x1E | Pole-Zero OpAmp bias |
| $I_{Bias\_V0T}$ | $D_{5..0}$ | 0x1C | 0T bias |

*Table 17: ICECAL channel control register (each channel has its own register). The hexadecimal default value is 7F-A0-29-13*

| Bits | Default | Function |
|---|---|---|

| | | |
|---|---|---|
| $Cint_{MSB}$ | 0x1 | 2 MSB of the integrator capacitor. |
| $Cint_{LSB0}$ | 0x7 | 3 LSB of the integrator capacitor for the subchannel 0. |
| $Cint_{LSB1}$ | 0x7 | 3 LSB of the integrator capacitor for the subchannel 1. |
| $IOff_{MSB}$ | 0xA | 4 MSB of the channel differential offset. |
| $IOff_{LSB0}$ | 0x0 | 2 LSB of the subchannel 0 differential offset. |
| $IOff_{LSB1}$ | 0x0 | 2 LSB of the subchannel 1 differential offset. |
| Zero | 0x5 | Filter zero controlled with 5 bit variable capacitor. |
| Pole | 0x8 | Filter pole controlled with 6 bit variable capacitor. |
| $Z_{In}$ | 0x13 | Input impedance controlled with 5 bits. |

*Table 18: Delay Line channel control register (hexadecimal default value = 00-11)*

| $D_{15..11}$ | $D_{10..6}$ | $D_{5..3}$ | $D_{2..1}$ | $D_0$ |
|---|---|---|---|---|
| $Phase_{ADC}$ | $Phase_{TH}$ | $Phase_{INT}$ | $L_{OCSEL}$ | $LVDS_{OEN}$ |

*Table 19: Delay Line channel control register function*

| Bits | Function |
|---|---|
| $Phase_{ADC}$ | ADC clock delay in ns.<br>Default value = 0x0 |
| $Phase_{TH}$ | Track&Hold clock delay in ns.<br>Default value = 0x0 |
| $Phase_{INT}$ | Integrator clock delay in ns. This clock signal is referenced to the Track&Hold clock. Hence, a 2-ns Integrator clock delay means 2 ns between Track&Hold clock rising/falling edge and Integrator clock rising/falling edge.<br>Default value = 0x2 |
| $L_{OCSEL}$ | LVDS clock output current selector.<br>• 0x0: 3.0 mA ($V_D$ = ±150 mV*).<br>• 0x1: 2.3 mA ($V_D$ = ±115 mV*).<br>• 0x2: 1.4 mA ($V_D$ = ±70 mV*).<br>• 0x3: 0.35 mA ($V_D$ = ±17.5 mV*).<br>Default value = 0x0. |
| $LVDS_{OEN}$ | This bit enables/disables the LVDS clock output that drives the ADC.<br>Default value = 0x1. |

*Considering LVDS termination resistor = 100 Ω.

### RELIABILITY ISSUES

As previously commented, TMR registers prevents from suffering SEUs. However, these serial TMR registers are only refreshed when SPI serial clock, $SPI_{SCLK}$ (pin 40), is switching. Therefore, if the same bit in a TMR register suffers two consecutive SEUs during a long idle period of the SPI bus (during data taking, for example), data might be corrupted.

To avoid long idle periods in the SPI bus, this chip is provided with an auxiliary input clock signal, $SPI_{Refresh}$ (41) to refresh TMR registers even when no SPI data is transferred. This feature can be enabled/disabled by changing the $!Clk_{Refresh\_EN}$ bit of the ICECAL main register. To not interfere with the normal operation of the serial registers, refresh clock switches only if the SPI slave is idle (see Figure 5).

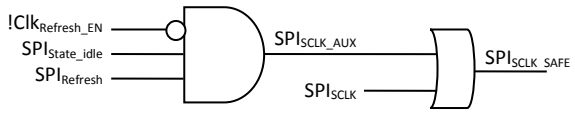



*Figure 7: SPI safe clock generation.*

# BIASING

### BIAS CURRENTS

The different bias currents used at each stage of the channel are exposed at the Table 20. A 6-bit DAC varies the current value (maximum value is mx135μA).

*Table 20: Biasing the different channel stages*

| Stage | Bias | p/n | x m | Value | Ib (μA) | IbMax (μA) |
|---|---|---|---|---|---|---|
| 0T | Ib | p | 6 | 30 | 435 | 810 |
| 0T | IbV | p | 1 | 28 | 75 | 135 |
| PZ | IbPZ | n | 3 | 30 | 210 | 405 |
| PZ | IbCEPZ | n | 4 | 17 | 390 | 540 |
| Int | IbInt | n | 3 | 30 | 210 | 405 |
| Int | IbCEInt | n | 4 | 28 | 300 | 540 |
| TH | IbTH | n | 3 | 30 | 210 | 405 |
| TH | IbCETH | n | 6 | 39 | 310 | 810 |
| OB | IbOB | p | 1 | 41 | 15 | 45 |

# POLE-ZERO FILTER

### ADJUSTMENT

The pole-zero filter can be adjusted through the pole and zero capacitors. The register values (see Table 17) and their frequency correspondence is pictured in

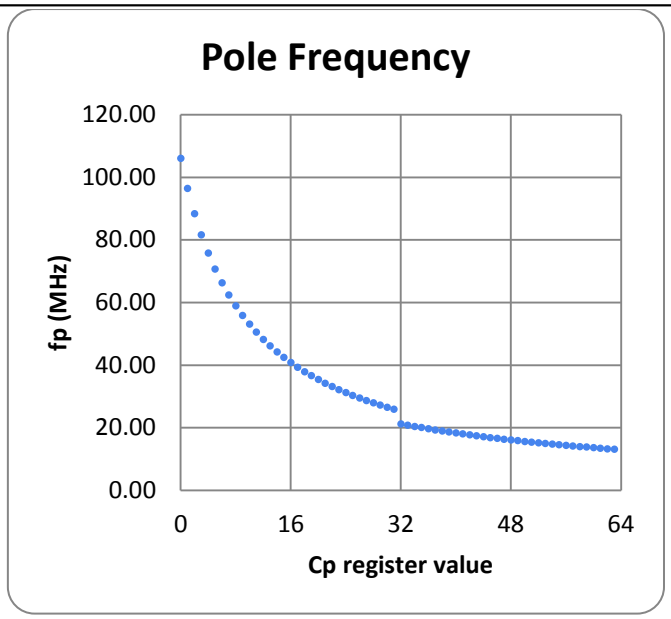



*Figure 8: Pole-zero filter pole frequency for each register value.*

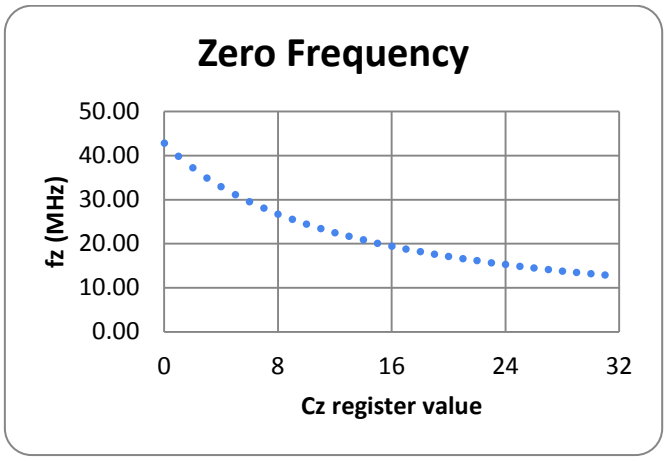



*Figure 9: Pole-zero filter zero frequency for each register value.*

# APPLICATIONS INFORMATION

## POWER SUPPLY DISTRIBUTION

The power distribution is based on a $V_{cc}$ (+3.3V). A decoupling capacitor network is used to filter the noise at the power supply. Place the lower values (1nF at each $V_{cc}$ pin) as close as possible to the chip in order to minimize the inductance of the path from ground to the power supply. Intermediate capacitor values (10nF and 100nF) are mounted between the device and the power source connector. Using the same package (0603 case) for all of these capacitors reduces the inductive performance of the decoupling circuit. Add tantalum capacitor (10µF) close to the power connector to minimize and filter the low frequency variations. A solid power plane reduces the resonances in the needed frequency range. The QFN64 package uses a central pad as a thermal pad, but in the ICECALv3 case, it is also used to ground the ASIC by using down bonds wires in order to minimize the bonding wire inductance. Place vias in the thermal pad to obtain a direct connection to the ground plane.

It is highly recommended to limit the current of the power supply following Table 21.

*Table 21: Typical and maximum power supply currents.*

| | $V_{CC}$ analog | $V_{CC}$ digital | $V_{ref}$ |
|---|---|---|---|
| Voltage (V) | 3.3 | 3.3 | 1.65 |
| Current limit (mA) | | | |
| Typical Current (mA) | 185 | 37 | 16 |

The operational limits for the power supplies and references are exposed in Table 22. Power supply or reference voltage values outside the expected region may result in

*Table 22: Typical and maximum power supply and reference voltage values.*

| Voltage source/reference | Minimum | Expected | Maximum |
|---|---|---|---|
| $V_{CC}$ analog (V) | 3.2 | 3.3 | 3.4 |
| $V_{CC}$ digital (V) | 3.2 | 3.3 | 3.4 |
| $V_{ref}$ (V) | 1.55 | 1.65 | 1.75 |
| $V_{coarse}$ (V) | 1.4 | 1.6 | 1.8 |

## BIAS VOLTAGE REFERENCE

The ICECALv3 is biased internally and current bias can be set in the main control register (Table 15). In order to reduce internal noise, the reference voltage generated internally for biasing is connected to an external pin which should be connected to a decoupling capacitor.

## INPUT VOLTAGE REFERENCE $V_{REF}$

$V_{ref}$ must be generated with a low output impedance source. The functioning of the first stage of the analog channel is very sensitive to noise and inductance from this reference. It is strongly recommended to use a 1nF decoupling capacitor at each pin and a plane for distribution (or local copper "pour") instead of simple wide paths.

Although the ideal is to generate the voltage source with an LDO, an alternative example of a circuit is shown in Figure 10. In the first example a band gap sets a voltage reference and is amplified before obtaining the desired $V_{ref}$. The value of the $R_s$ needs to be studied in detail to avoid stability problems of the amplifier and to be able to have enough current to feed the chip. In this example is important to verify that the amplifier output current can achieve 16mA per ICECAL chip.

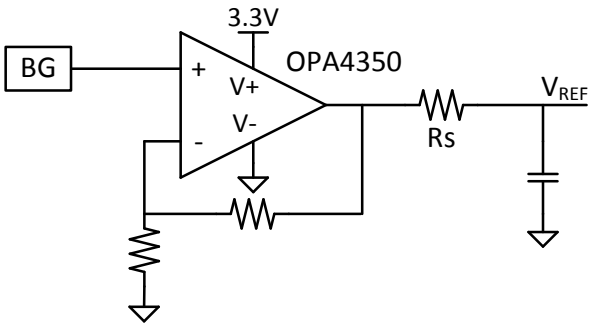



*Figure 10: $V_{ref}$ generation examples.*

## COMMON MODE $V_{CM}$

All common mode levels can be connected to a common $V_{CM}$ of 1.5V. This voltage can be with an operational amplifier like the Vref, although the current consumption is very little and Rs can be higher for stability purposes. It is recommended to use one 1nF capacitor at each $V_{CM}$ pin.

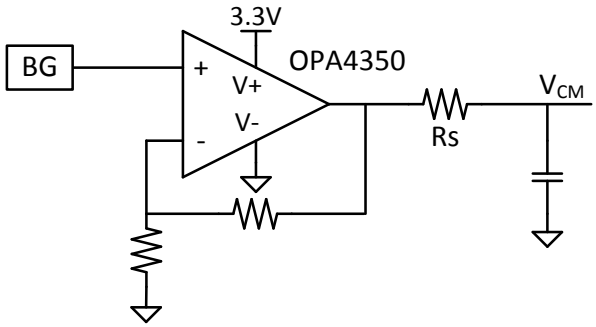



*Figure 11: $V_{CM}$ generation with an operational amplifier.*

## INPUT

Each ICECALv3 input requires an AC coupling and a parallel resistor with another AC coupling to ground. Use four optionally capacitors in parallel (100pF, 1nF, 10nF and 100nF) to get a wide bandwidth frequency

range at each input signal pin for high precision performances. The differential ICECAL have a double input signal (I+ and I-), but it is only used the I- one, and **the input signal must be a negative pulse**.

Tests at lab showed that the inputs of the ICECAL are sensible to ESD effects. Following the classification in , the expected classification is 1C or even 2.

*Table 23: : HBM ESD Component Classification Levels (ANSI/ESDA/JEDEC JS-001-2010)*

| Classification | Voltage Range (V) |
|---|---|
| **0** | < 250 |
| **1A** | 250 to < 500 |
| **1B** | 500 to < 1000 |
| **1C** | 1000 to < 2000 |
| **2** | 2000 to < 4000 |
| **3A** | 4000 to < 8000 |
| **3B** | ≥ 8000 |

As a consequence, we recommend the use of an input protection circuit as presented in Figure 10:

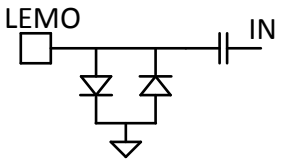



*Figure 12: Input protection circuit*

## OUTPUT

The differential outputs are a low impedance output. Each one requires also AC coupling (like the AC coupling circuit for the input signals) to adapt to the ADC input voltage levels. The circuit presented in Figure 12 shows an example of the interface between the ICECAL outputs to the ADC inputs. The ADC used is the AD9238. The circuit includes the AC coupling (with three different capacitor values to minimize their inductance behavior), a low pass filter to reduce noise and voltage dividers using the ADC references to fix the offset of the ADC (and maximize the ADC range).

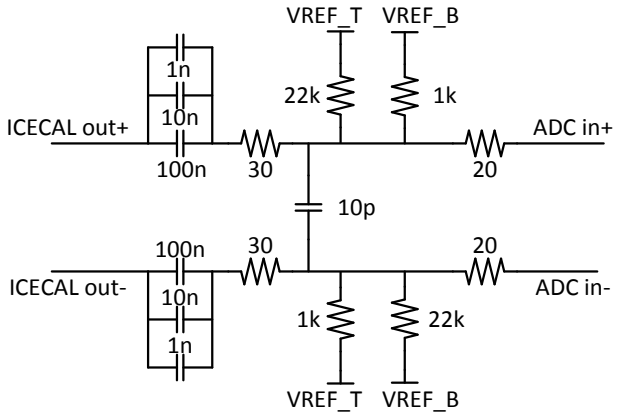



*Figure 13: ICECAL to ADC circuit example.*

In the example exposed, the ADC should be configured as following:

*Table 24: ADC AD9238 recommended configuration.*

| Pin No. | Mnemonic | Description | Voltage |
|---|---|---|---|
| 6 | REFT_A | Differential Reference (+) for Channel A. | 2.25V |
| 7 | REFB_A | Differential Reference (−) for Channel A. | 1.25V |
| 8 | VREF | Voltage Reference Input/Output. | 1V |
| 9 | SENSE | Reference Mode Selection. | 0V |
| 10 | REFB_B | Differential Reference (−) for Channel B. | 1.25V |
| 11 | REFT_B | Differential Reference (+) for Channel B. | 2.25V |
| 19 | DCS | Enable Duty Cycle Stabilizer (DCS) Mode (Tie High to Enable). | High |
| 20 | DFS | Data Output Format Select Bit (Low for Offset Binary, High for Twos Complement). | Low |
| 21 | PDWN_B | Power-Down Function Selection for Channel B:<br>• Logic 0 enables Channel B.<br>• Logic 1 powers down Channel B. (Outputs static, not High-Z.) | Low |
| 22 | OEB_B | Output Enable Bit for Channel B:<br>• Logic 0 enables Data Bus B.<br>• Logic 1 sets outputs to High-Z. | Low |
| 59 | OEB_A | Output Enable Bit for Channel A:<br>• Logic 0 enables Data Bus A.<br>• Logic 1 sets outputs to High-Z. | Low |
| 60 | PDWN_A | Power-Down Function Selection for Channel A:<br>• Logic 0 enables Channel A.<br>• Logic 1 powers down Channel A. (Outputs static, not High-Z.) | Low |
| 61 | MUX_SELECT | Data Multiplexed Mode (high setting disables output data multiplexed mode). | High |
| 62 | SHARED_REF | Shared Reference Control Bit (Low for Independent Reference Mode, High for Shared Reference Mode). | Low |

### DLL $V_{CONTROL}$

It is recommended to use a voltage divider to read the DLL $V_{CONTROL}$ and adapt the voltage range to the ADC input.

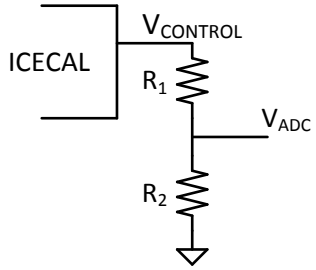



*Figure 14: Voltage divider to adapt the voltage to the ADC input range.*

### DLL $V_{COARSE}$

The input $V_{COARSE}$ voltage has to be fixed. Its expected value is 1.2V, but the range should cover from 0.5V to 2V.

In the FEB of the Calorimeter Upgrade, the input will be driven by the GBT_SCA DAC with a range from 0 to 1V. It is recommended to use an operational amplifier (Figure 14) to increase the DAC output voltage range by a factor 2 or 2.5.

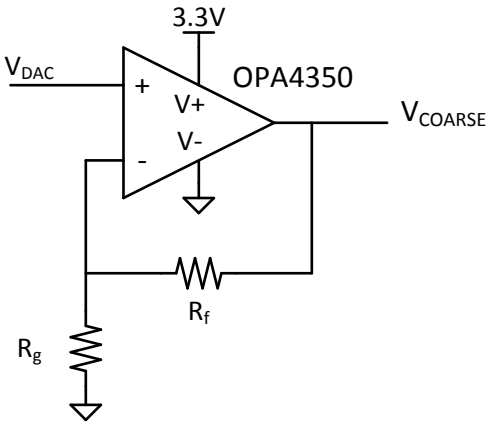



*Figure 15: circuit to increase the $V_{COARSE}$ range.*

### SPI MISO

The SPI MISO signal requires an external 500Ω pull-up resistor connected to the same high voltage value as the reading system.

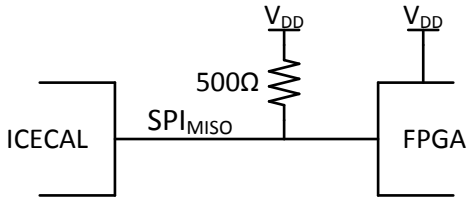



*Figure 16: SPI MISO signal requires a 500Ω pull-up resistor.*

# LAYOUT

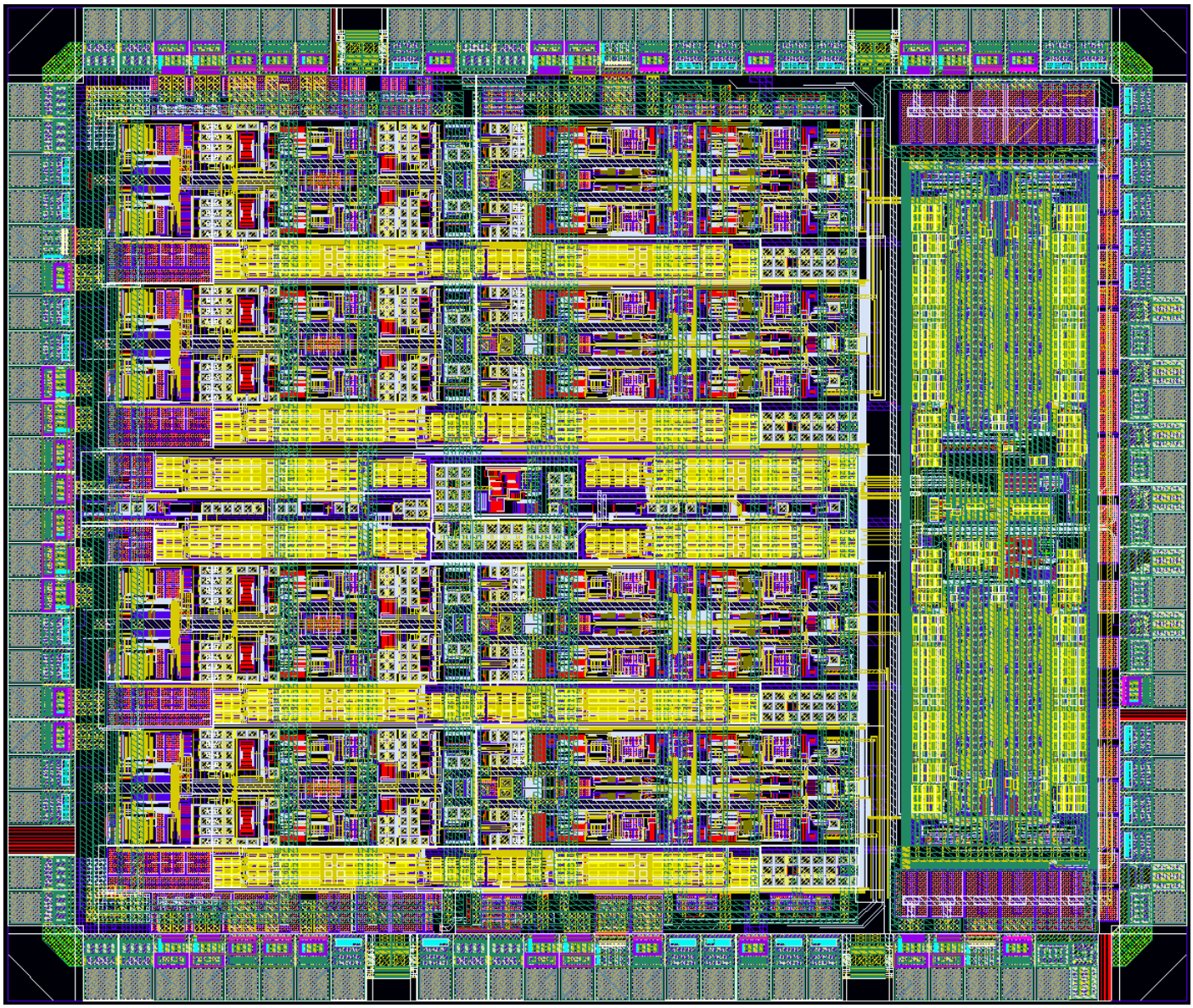


**Figure 17: ICECALv3 Layout picture**

## BONDING DIAGRAM

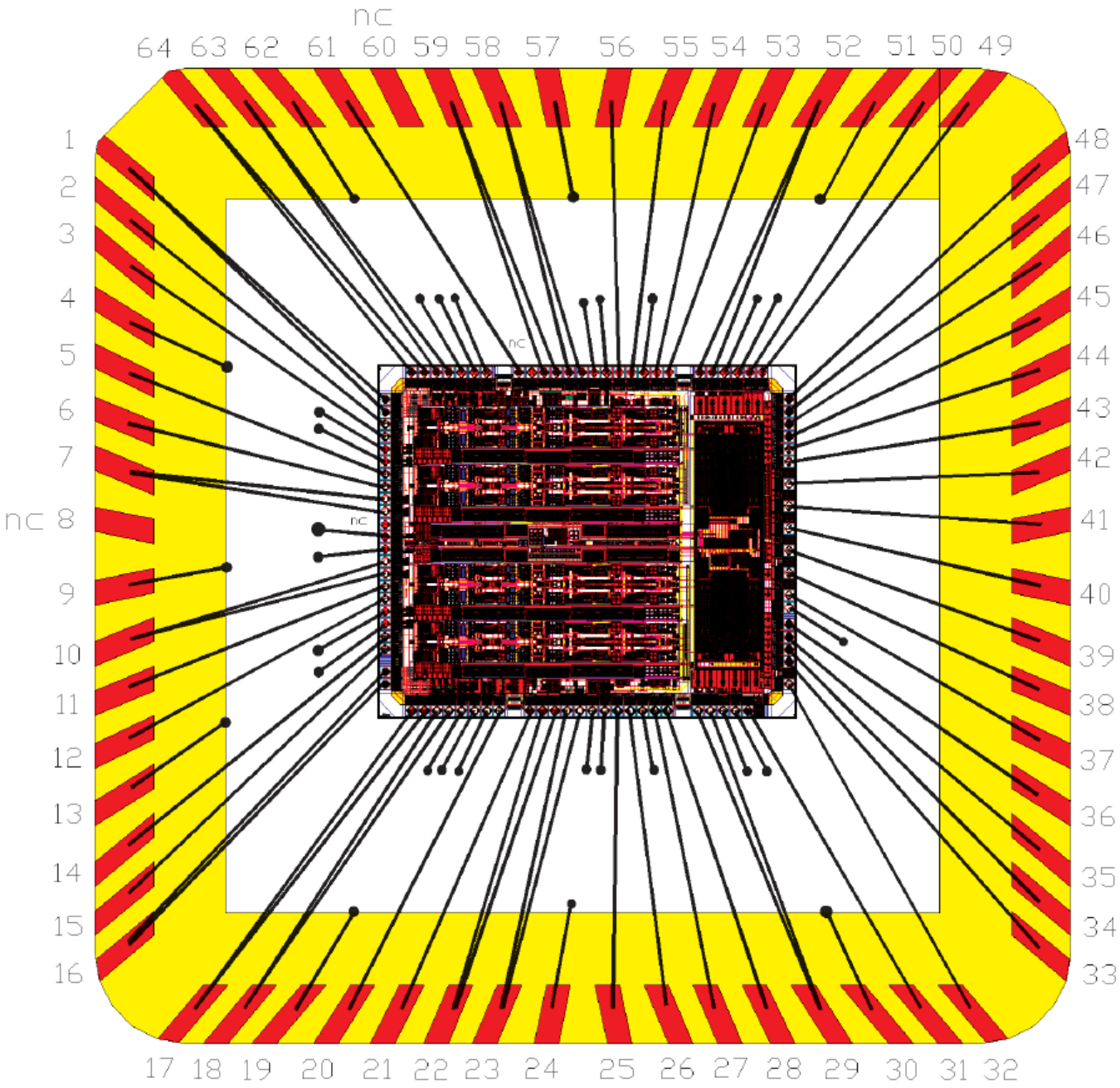



*Figure 61. ICECALv3 Bonding Diagram with the DIE ground pads connected to the central package pad.*

# OUTLINE DIMENSIONS

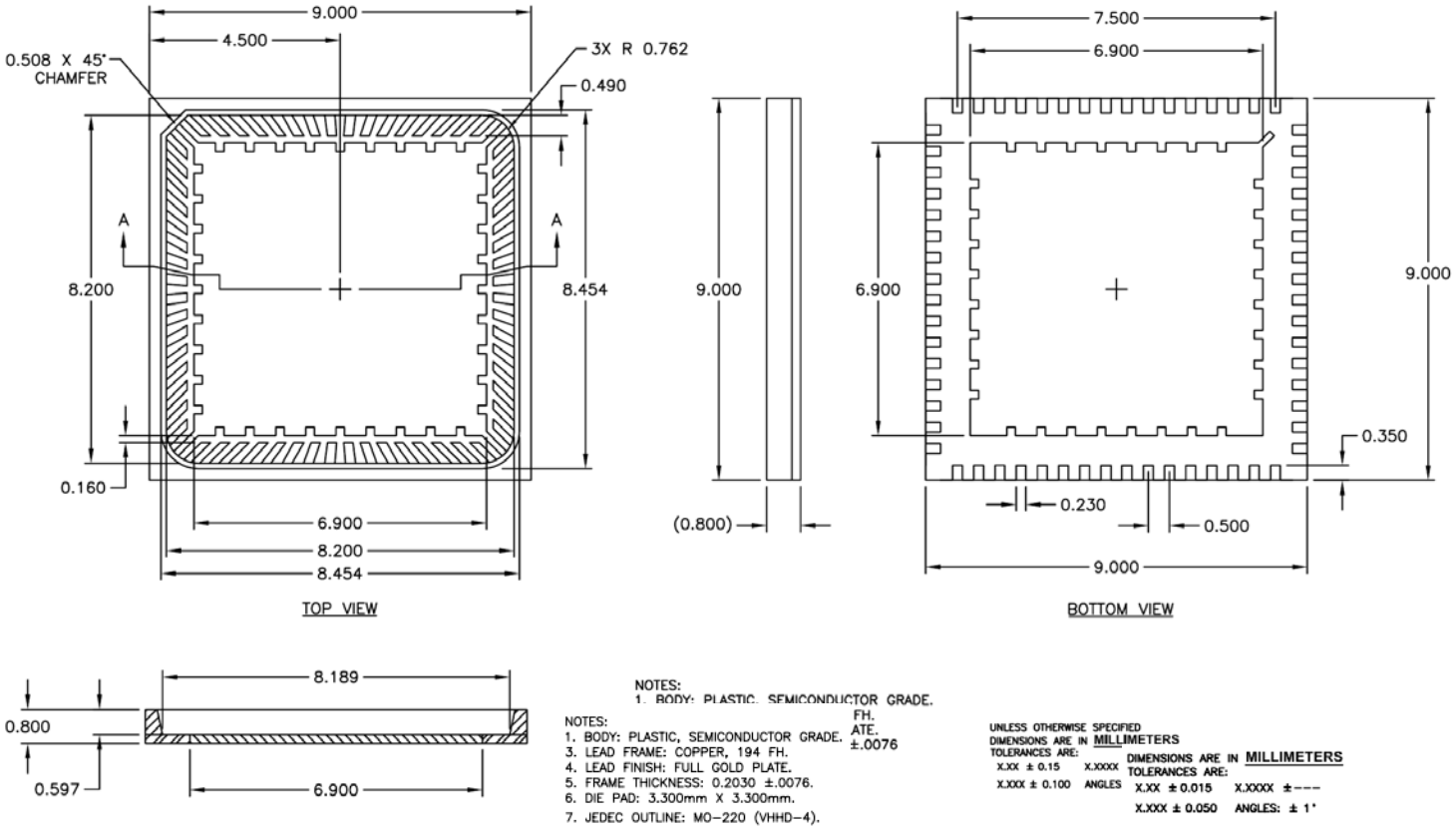



*Figure 62. 64-Lead QFN packaging outline. Dimensions shown in millimeters. Packaging provided by SEMPAC, INC.*

# ORDERING GUIDE

| Model | Temperature Range[1] | Package Description[2,3] |
|---|---|---|
| ICECALv3 | −40°C to +125°C | 64-Lead QFN |

[1] Temperature range for the ASIC technology used. To be tested at the next document revisions.
[2] Package dimensions without lid: 9 x 9 mm, 0.8 mm thick.
[3] Lid dimensions 9 x 9 mm, 0.2 mm thick.

# NOTES



Institut de Ciències del Cosmos